= Short Datasheet =

AK09911

3-axis Electronic Compass

1. Features

- □ A 3-axis electronic compass IC with high sensitive Hall sensor technology.
- □ Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

- □ Functions:
  - 3-axis magnetometer device suitable for compass application
  - Built-in A to D Converter for magnetometer data out
  - 14-bit data out for each 3-axis magnetic component
    - ➢ Sensitivity: 0.6 μT/LSB (typ.)
  - Serial interface
    - ➢ I^2C bus interface
      Standard, Fast and High-speed mode (up to 2.5 MHz) compliant with Philips I2C specification Ver.2.1
  - Operation mode
    - ➢ Power-down, Single measurement, Continuous measurement, Self-test and Fuse ROM access
  - DRDY function for measurement data ready
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Power on Reset circuit
  - Self test function with internal magnetic source

- □ Operating temperatures:
  - -30˚C to +85˚C
- □ Operating supply voltage:
  - Analog power supply +2.4V to +3.6V
  - Digital Interface supply +1.65V to analog power supply voltage
- □ Current consumption:
  - Power-down: 3 μA (typ.)
  - Measurement:
    - ➢ Average current consumption at 100 Hz repetition rate: 2.4 mA (typ.)

- □ Package:
  - AK09911C 8-pin WL-CSP (BGA): 1.2 mm × 1.2 mm × 0.5 mm (typ.)

2. Overview

AK09911 is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK09911 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK09911 has the following features:

(1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.

(2) Wide dynamic measurement range and high resolution with lower current consumption.
  - Output data resolution: 14-bit (0.6 µT/LSB)
  - Measurement range: ±4900 µT
  - Average current at 100 Hz repetition rate: 2.4 mA (typ.)

(3) Digital serial interface
  - I^2C bus interface to control AK09911 functions and to read out the measured data by external CPU. A dedicated power supply for I^2C bus interface can work in low-voltage apply as low as 1.65V.

(4) DRDY register informs to system that measurement is end and set of data in registers are ready to be read.

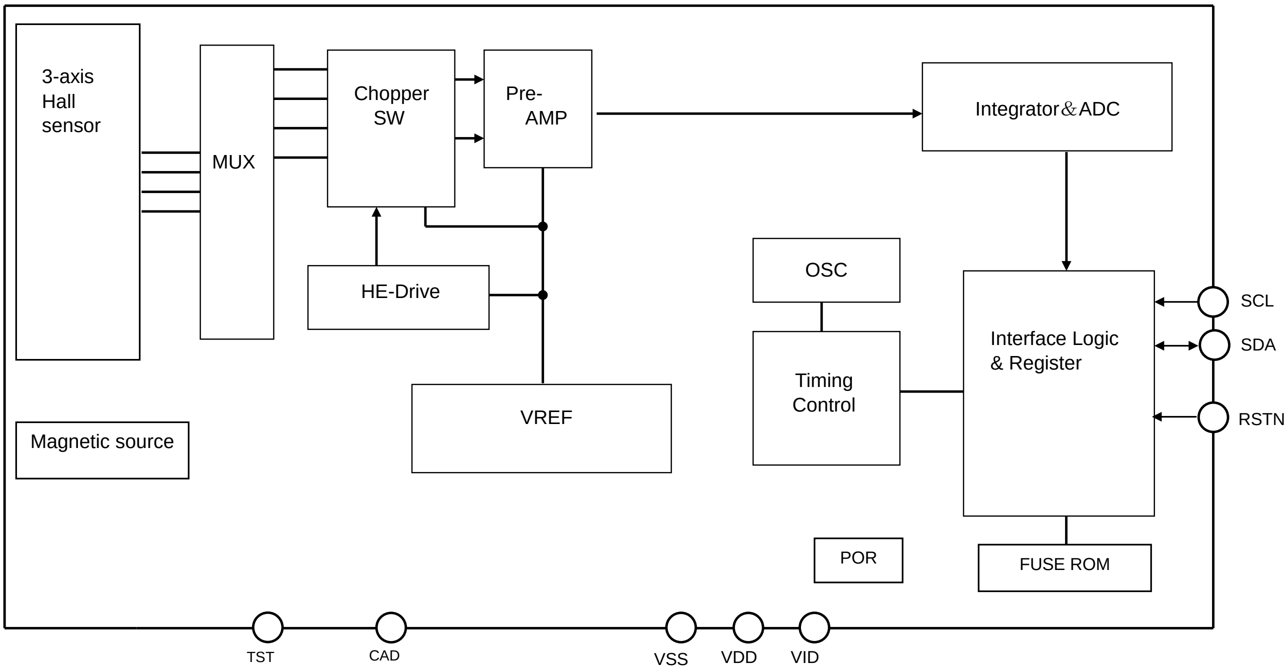
(5) Device is worked by on-chip oscillator so no external clock source is necessary.

(6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

3. Table of Contents

4. Circuit Configration

4.1. Block Diagram



4.2. Block Function

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor.
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Intergrator & ADC	Integrates and amplifies pre-AMP output and performs analog-to-digital conversion.
OSC	Generates an operating clock for sensor measurement.
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
VREF	Generates reference voltage and current.
Interface Logic & Register	Exchanges data with an external CPU. I2C bus interface using two pins, namely, SCL and SDA. Standard, Fast and High-speed modes are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC.
Magnetic Source	Generates magnetic field for self test of magnetic sensor.
FUSE ROM	Fuse for adjustment.

4.3. Pin Function

Pin No.	Pin name	I/O	Power supply	Type	Function
A1	VDD	-	-	Power	Positive power supply pin.
A2	CAD	I	VDD	CMOS	Slave address input pin. Connect to VSS or VDD,
A3	TST	I/O	VDD	CMOS	Test pin. Pulled down by 100kΩ internal resister. Keep this pin electrically non-connected.
B1	VSS	-	-	Power	Ground pin.
B3	SCL	I	VID	CMOS	Control data clock input pin Input: Schmidt trigger
C1	VID	-	-	Power	Digital interface positive power supply pin.
C2	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to “L”.
C3	SDA	I/O	VID	CMOS	Control data input/output pin Input: Schmidt trigger, Output: Open drain

5. Overall Characteristics

5.1. Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (Vdd, Vid)	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+) +0.3	V
Input current	IIN	-	±10	mA
Storage temperature	Tst	-40	+125	˚C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

5.2. Recommended Operating Conditions

Vss=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	˚C
Power supply voltage	VDD pin voltage	Vdd	2.4	3.0	3.6	V
	VID pin voltage	Vid	1.65		Vdd	V

5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd=2.4V to 3.6V, Vid=1.65V to Vdd, Temperature range=-30˚C to 85˚C

5.3.1. DC Characteristics

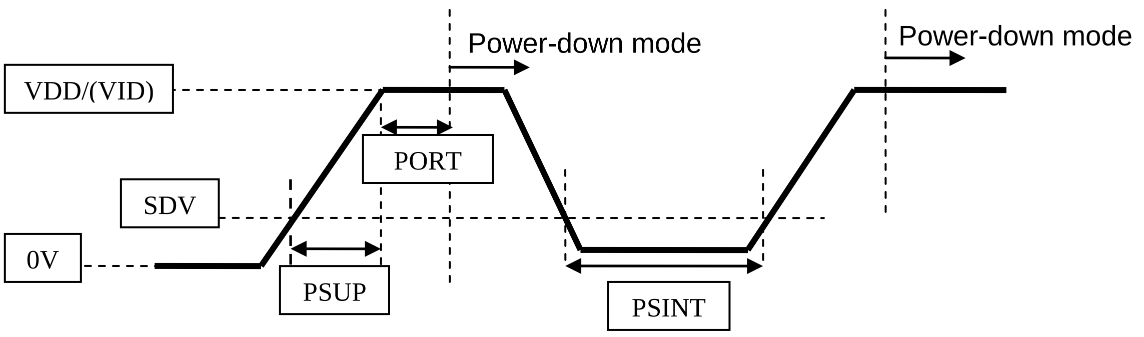
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	RSTN		70%Vid		Vid+0.3	V
		SCL SDA		70%Vid			
Low level input voltage 1	VIL1	RSTN SCL SDA		-0.3		30%Vid	V
High level input voltage 2	VIH2	TST CAD		70%Vdd		Vdd+0.3	V
Low level input voltage 2	VIL2			-0.3		30%Vdd	V
Input current 1	IIN1	RSTN SCL SDA	Vin=Vss or Vid	-10		+10	μA
		CAD	Vin=Vss or Vdd	-10		+10	
Input current 2	IIN2	TST	Vin=Vdd			100	μA
Hysteresis input voltage (Note 2)	VHS	SCL SDA	Vid≥2V	5%Vid			V
			Vid<2V	10%Vid			
Low level output voltage (Note 3)	VOL	SDA	IOL≤+3mA Vid≥2V			0.4	V
			IOL≤+3mA Vid<2V			20%Vid	
Current consumption (Note 4)	IDD1	VDD VID	Power-down mode Vdd=Vid=3.0V		3	6	μA
	IDD2		When magnetic sensor is driven		3	6	mA
	IDD3		Self-test mode		5	8	mA
	IDD4		(Note 5)		0.1	5	μA

(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Output is open-drain. Connect a pull-up resistor externally. Maximum capacitive load: 400pF (Capacitive load of each bus line for I2C bus interface).
(Note 4) Without any resistance load. It does not include the current consumed by external loads (pull-down resister, etc.). RSTN, SDA, SCL = Vid or 0V. CAD = Vdd or 0V.
(Note 5) (case 1) Vdd=ON, Vid=ON, RSTN pin = “L”. (case 2) Vdd=ON, Vid=OFF (0V), RSTN pin = “L”. (case 3) Vdd=OFF (0V), Vid=ON.

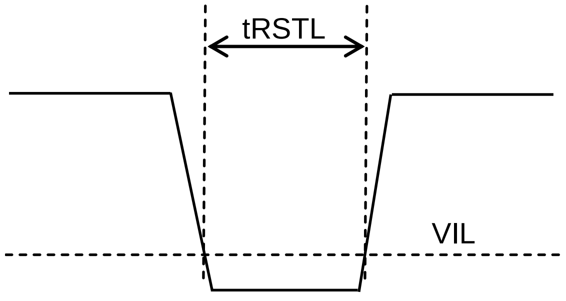
5.3.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 6)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid).			50	ms
POR completion time (Note 6)	PORT		Period of time after PSUP to Power-down mode (Note 7)			100	μs
Power supply turn off voltage (Note 6)	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 7)			0.2	V
Power supply turn on interval (Note 6)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 7)	100			μs
Wait time before mode setting	Twat			100			μs

(Note 6) Reference value for design.
(Note 7) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK09911 transits to Power-down mode.



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset input effective pulse width (“L”)	tRSTL	RSTN		5			μs



5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT		-	14	-	bit
Time for measurement	TSM	Single measurement mode		7.2	8.5	ms
Magnetic sensor sensitivity (Note 8)	BSE	Tc = 25 ˚C	0.57	0.6	0.63	μT/LSB
Magnetic sensor measurement range (Note 9)	BRG	Tc = 25 ˚C	±4912			μT
Magnetic sensor initial offset (Note 10)		Tc = 25 ˚C	-500		+500	LSB

(Note 8) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM.
(Note 9) Reference value for design
(Note 10) Value of measurement data register on shipment without applying magnetic field on purpose.

5.3.4. I²C Bus Interface

I²C bus interface is compliant with Standard mode, Fast mode and High-speed mode. Standard/Fast mode is selected automatically by fSCL.

☐ Standard mode

fSCL≤100kHz

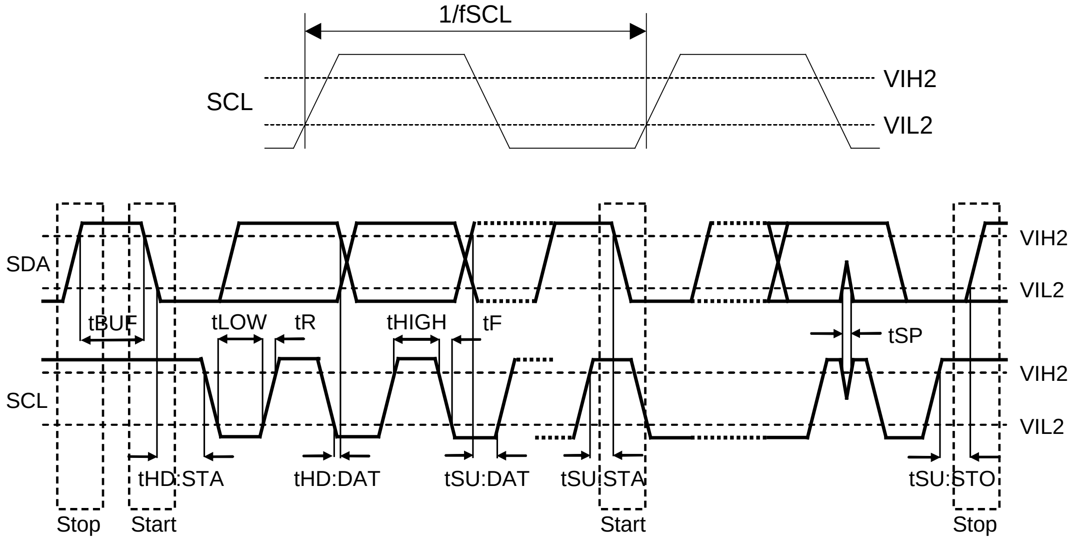
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock “High” time	4.0			μs
tLOW	SCL clock “Low” time	4.7			μs
tR	SDA and SCL rise time			1.0	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	4.0			μs
tSU:STA	Start Condition setup time	4.7			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

☐ Fast mode

100Hz≤fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock “High” time	0.6			μs
tLOW	SCL clock “Low” time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μs
tSP	Noise suppression pulse width			50	ns

[I²C bus interface timing]



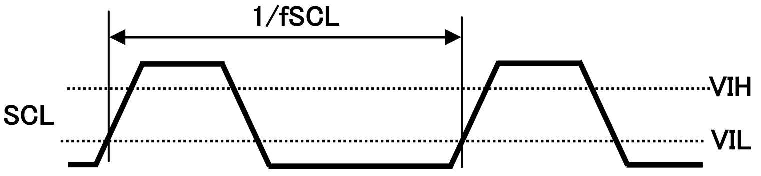
- High-speed mode (Hs-mode)
  - $C_b \leq 100pF$ (C_b: load capacitance)
    fSCLH≤2.5MHz

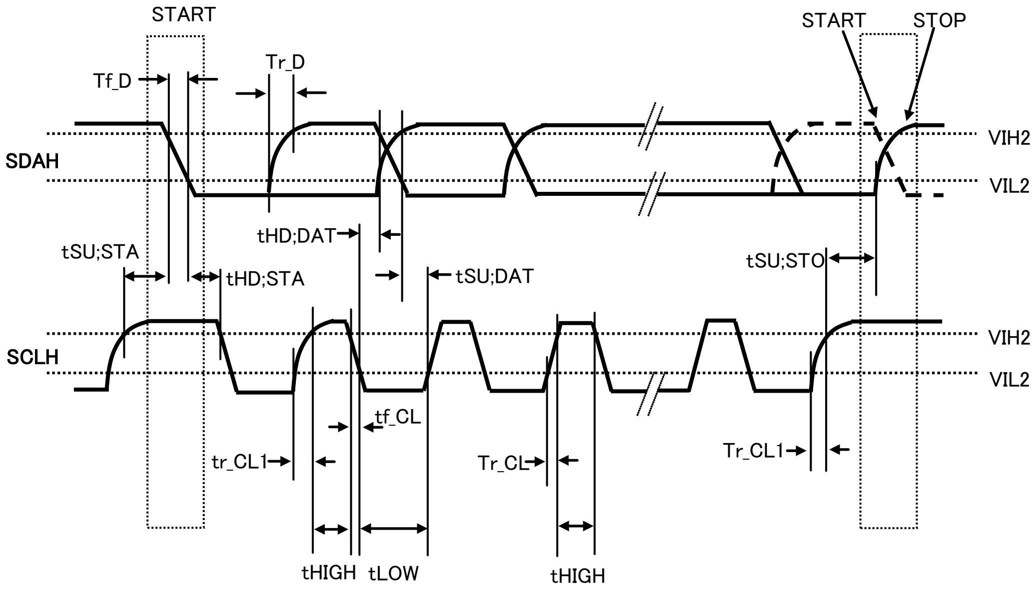
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			2.5	MHz
tHIGH	SCLH clock “High” time	110			ns
tLOW	SCLH clock “Low” time	220			ns
tR_CL	SCLH rise time	10		40	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	10		80	ns
tR_DA	SDAH rise time	10		80	ns
tF_CL	SCLH fall time	-		40	ns
tF_DA	SDAH fall time	-		80	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

  - $C_b \leq 400pF$
    fSCLH≤1.7MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			1.7	MHz
tHIGH	SCLH clock “High” time	120			ns
tLOW	SCLH clock “Low” time	320			ns
tR_CL	SCLH rise time	20		80	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	20		160	ns
tR_DA	SDAH rise time	20		160	ns
tF_CL	SCLH fall time	-		80	ns
tF_DA	SDAH fall time	-		160	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

[I^{2}C bus interface timing of Hs-mode]





6. Function Explanation

6.1. Power States

When VDD and VID are turned on from Vdd=OFF (0V) and Vid=OFF (0V), all registers in AK09911 are initialized by POR circuit and AK09911 transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 6.1. Power state

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V). It doesn’t affect external interface.Digital input pins other than SCL and SDA pin should be fixed to “L”(0V).
2	OFF (0V)	1.65V to 3.6V	OFF (0V) It doesn’t affect external interface.
3	2.4V to 3.6V	OFF (0V)	OFF(0V) It doesn’t affect external interface. Digital input pins other than SCL and SDA pin should be fixed to “L”(0V).
4	2.4V to 3.6V	1.65V to Vdd	ON

6.2. Reset Functions

When the power state is ON, always keep Vid≤Vdd.
Power-on reset (POR) works until Vdd reaches to the operation effective voltage (about 1.1V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to Power-down mode.

When Vdd=2.4 to 3.6V, POR circuit and VID monitor circuit are active. When Vid=0V, AK09911 is in reset status and it consumes the current of reset state (IDD4).

AK09911 has four types of reset;

(1) Power on reset (POR)
When Vdd rise is detected, POR circuit operates, and AK09911 is reset.

(2) VID monitor
When VID is turned OFF, AK09911 is reset.

(3) Reset pin (RSTN)
AK09911 is reset by Reset pin. When Reset pin is not used, connect to VID.

(4) Soft reset
AK09911 is reset by setting SRST bit. When AK09911 is reset, all registers are initialized and AK09911 transits to Power-down mode.

6.3. Operation Mode

AK09911 has following nine operation modes:

(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode 1
(4) Continuous measurement mode 2
(5) Continuous measurement mode 3
(6) Continuous measurement mode 4
(7) Self-test mode
(8) Fuse ROM access mode

By setting CNTL2 register MODE[4:0] bits, the operation set for each mode is started.
A transition from one mode to another is shown below.

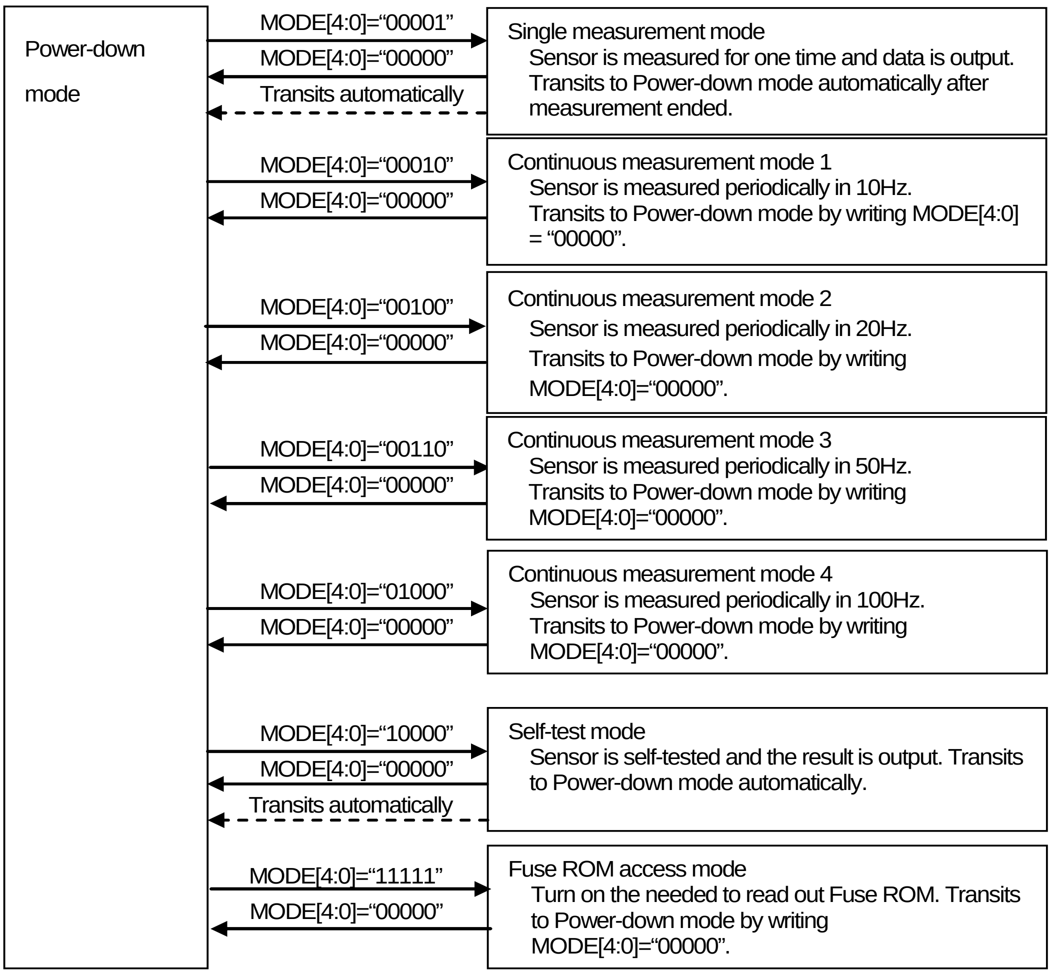
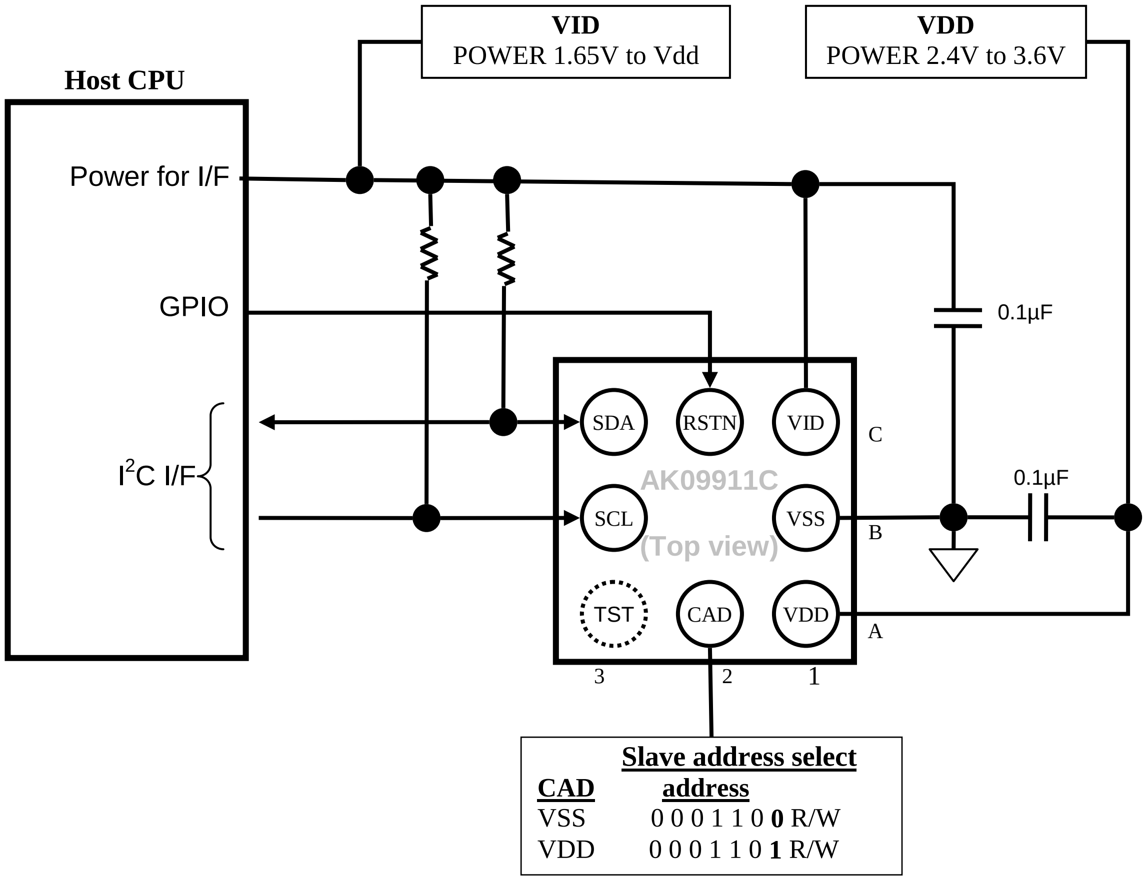


Figure 6.1. Operation mode

When power is turned ON, AK09911 is in Power-down mode. When a specified value is set to MODE[4:0], AK09911 transits to the specified mode and starts operation. When user wants to change operation mode, transit to Power-down mode first and then transit to other modes. After Power-down mode is set, at least 100 μs (Twat) is needed before setting another mode

7. Example of Recommended External Connection

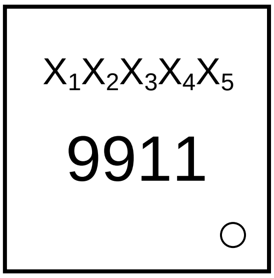


Pins of dot circle should be kept non-connected.

8. Package

8.1. Marking

- ☐ Date code: $X_1X_2X_3X_4X_5$
  - X1 = ID
  - X2 = Year code
  - X3X4 = Week code
  - X5 = Lot
- ☐ Product name: 9911



<Top view>

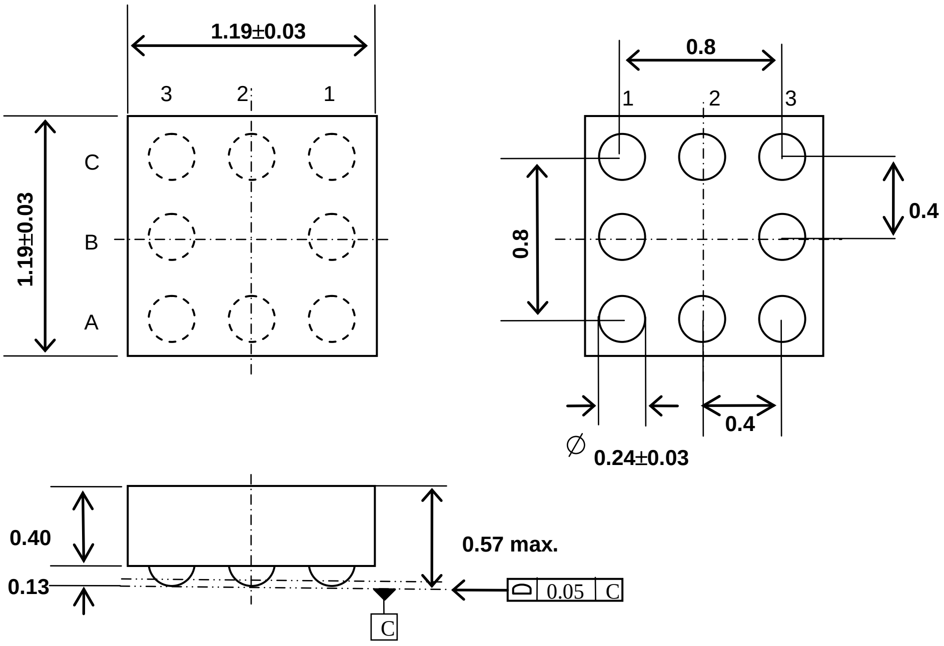
8.2. Pin Assignment

	3	2	1
C	SDA	RSTN	VID
B	SCL		VSS
A	TST	CAD	VDD

<Top view>

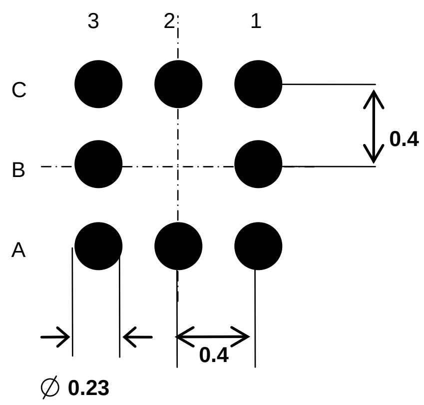
8.3. Outline Dimensions

[mm]



8.4. Recommended Foot Print Pattern

[mm]



9. Relationsip between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.